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10/791,094	03/01/2004	Darin A. Chan	H1844	2464

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EXAMINER	
QUINTO, KEVIN V	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/791,094	CHAN ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11,13-16 and 18-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16 and 18-24* is/are allowed.

6)☒ Claim(s) *1,3-11 and 13-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 3-11, and 13-15 have been considered but are moot in view of the new ground(s) of rejection.

2. The examiner notes newly amended claims 7-10 and thus hereby withdraws the rejections of claims 7-10 made under 35 USC § 112 in the previous Office action.

3. The examiner notes newly amended claims 8 and 9; however newly amended claims 1 and 6 have lead to a double patenting warning for claims 6, 8, 9, and 10.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 6-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 6 recites the limitation "the insulating sidewall spacer" in lines 8 and 9 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1, 3, 11, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Chau et al. (USPN 6,518,155 B1).

9. In reference to claims 1 and 11, Chau et al. (USPN 6,518,155 B1, hereinafter referred to as the "Chau" reference) discloses a similar device and its method of fabrication. Figure 2 of Chau illustrates an integrated circuit while figures 3A-3I illustrate the process for forming it. Figures 2, 3A-3I show an integrated circuit with a gate dielectric layer (318) on a semiconductor substrate (300). There is a gate (320) on the gate dielectric layer (318). There is an insulating sidewall spacer (330) around the gate (318). There are source/drain junctions (331) in the semiconductor substrate (300). Silicide (336) is formed on the source/drain junctions (331) and the gate (320). There are trenches in the semiconductor substrate (300) around the outer edge of the insulating sidewall spacer (330). Although not shown, it is understood that an interlayer dielectric is formed above the semiconductor substrate (300) and that contacts are formed in the interlayer dielectric which contact the silicide (336) in order to take advantage of the low resistance silicide.

10. With regard to claim 3, Chau states (column 6, lines 47-49) that the etching process to form the trench uses an etching process that etches the semiconductor substrate (300). This is also illustrated in figure 3F.

11. In reference to claim 13, the trenches extend into the semiconductor substrate (330) to a level lower than the silicide (336).

12. Claims 6 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Chau (USPN 6,518,155 B1).

13. So far as understood in claims 6 and 8, Chau (USPN 6,518,155 B1) discloses a similar device and its fabrication method. Figure 2 of Chau illustrates an integrated circuit while figures 3A-3I illustrate the process for forming it. Figures 2, 3A-3I show an integrated circuit with a gate dielectric layer (318) on a semiconductor substrate (300). There is a gate (320) on the gate dielectric layer (318). There are source/drain junctions (331) in the semiconductor substrate (300). Silicide (336) is formed on the source/drain junctions (331) and the gate (320). There is an insulating spacer (330) around the gate (320). There are trenches in the semiconductor substrate (300) at the outer edge of the sidewall spacer (330). Chau makes it clear (column 6, lines 47-49 and in figures 3F) that the trenches are formed by an etching process that etches a semiconductor substrate (1). Although not shown, it is understood that an interlayer dielectric is formed above the semiconductor substrate (300) and that contacts are formed in the interlayer dielectric which contact the silicide (336) in order to take advantage of the low resistance silicide.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chau (USPN 6,518,155 B1) in view of Russell et al. (USPN 5,648,175).

16. In reference to claim 4, Chau does not explicitly disclose the use of a low dielectric constant interlayer dielectric. However the use of such a material is well known in the art. Russell et al. (USPN 5,648,175, hereinafter referred to as the "Russell" reference) discloses that BPSG (borophosphosilicate glass) is desirable for use as an interlayer dielectric since it has the benefits of a low dielectric constant, low stress, and good adhesion properties (column 1, lines 27-30). Russell discloses that these qualities are desirable in the art (column 1, lines 41-44). In view of Russell, it would therefore be obvious to use a low dielectric constant interlayer dielectric in the device of Chau in order to attain these benefits.

17. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chau (USPN 6,518,155 B1) in view of Merrill (USPN 5,918,141) as applied to claim 1 above and further in view of Sekiguchi (USPN 6,333,255 B1).

18. In reference to claim 4, Chau does not explicitly disclose the use of a low dielectric constant interlayer dielectric. However the use of such a material is well known in the art. Sekiguchi (USPN 6,333,255 B1) discloses that low dielectric constant materials, such as HSQ and Teflon-AF, are desirable for use as an interlayer dielectric since it has the benefits of a low dielectric constant which leads to the possibility of a smaller device (column 1, lines 35-46). The attainment of a smaller semiconductor

device is a known goal in the art (column 1, lines 10-15). In view of Sekiguchi, it would therefore be obvious to use a low dielectric constant interlayer dielectric in the device of Chau in order to attain these benefits.

19. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chau (USPN 6,518,155 B1) in view of Liauh (USPN 5,027,185) and further in view of Wald et al. (USPN 5,932,491).

20. In reference to claim 5, Chau does not disclose the exact material which is used for the contact. However Liauh (USPN 5,027,185) discloses that in the semiconductor art, contacts are formed with low resistance as a desired goal (column 1, lines 38-57). Wald et al. (USPN 5,932,491, hereinafter referred to as the "Wald" reference) discloses the use of titanium, tungsten, and alloys thereof in a contact since they have a low resistance (column 5, lines 45-48). In view of Liauh and Wald, it would therefore be obvious to use titanium, tungsten, and its alloys as contacts in order to gain the benefit of a low resistance contact.

21. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chau (USPN 6,518,155 B1) in view of Liauh (USPN 5,027,185) and further in view of Yoshida et al. (USPN 6,580,143 B2).

22. In reference to claim 5, Chau does not disclose the exact material which is used for the contact. However Liauh (USPN 5,027,185) discloses that in the semiconductor art, contacts are formed with low resistance as a desired goal (column 1, lines 38-57). Yoshida et al. (USPN 6,580,143 B2, hereinafter referred to as the "Yoshida" reference) discloses that gold, silver, and titanium have a low resistance (column 4, lines 11-16).

In view of Liauh and Yoshida, it would therefore be obvious to gold, silver, and titanium as contacts in order to gain the benefit of a low resistance contact.

23. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chau (USPN 6,518,155 B1) in view of Russell et al. (USPN 5,648,175).

24. So far as understood in claim 9, Chau does not explicitly disclose the use of a low dielectric constant interlayer dielectric. However the use of such a material is well known in the art. Russell (USPN 5,648,175) discloses that BPSG (borophosphosilicate glass) is desirable for use as an interlayer dielectric since it has the benefits of a low dielectric constant, low stress, and good adhesion properties (column 1, lines 27-30). Russell discloses that these qualities are desirable in the art (column 1, lines 41-44). In view of Russell, it would therefore be obvious to use a low dielectric constant interlayer dielectric in the device of Chau in order to attain these benefits.

25. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chau (USPN 6,518,155 B1) in view of Sekiguchi (USPN 6,333,255 B1).

26. So far as understood in claim 9, Chau does not explicitly disclose the use of a low dielectric constant interlayer dielectric. However the use of such a material is well known in the art. Sekiguchi (USPN 6,333,255 B1) discloses that low dielectric constant materials, such as HSQ and Teflon-AF, are desirable for use as an interlayer dielectric since it has the benefits of a low dielectric constant which leads to the possibility of a smaller device (column 1, lines 35-46). The attainment of a smaller semiconductor device is a known goal in the art (column 1, lines 10-15). In view of Sekiguchi, it would

therefore be obvious to use a low dielectric constant interlayer dielectric in the device of Chau in order to attain these benefits.

27. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chau (USPN 6,518,155 B1) in view of Liauh (USPN 5,027,185) and further in view of Wald et al. (USPN 5,932,491).

28. So far as understood in claim 10, Chau does not disclose the exact material which is used for the contact. However Liauh (USPN 5,027,185) discloses that in the semiconductor art, contacts are formed with low resistance as a desired goal (column 1, lines 38-57). Wald et al. (USPN 5,932,491, hereinafter referred to as the "Wald" reference) discloses the use of titanium, tungsten, and alloys thereof in a contact since they have a low resistance (column 5, lines 45-48). In view of Liauh and Wald, it would therefore be obvious to use titanium, tungsten, and its alloys as contacts in order to gain the benefit of a low resistance contact.

29. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chau (USPN 6,518,155 B1) in view of Liauh (USPN 5,027,185) and further in view of Yoshida et al. (USPN 6,580,143 B2).

30. So far as understood in claim 10, Chau does not disclose the exact material which is used for the contact. However Liauh (USPN 5,027,185) discloses that in the semiconductor art, contacts are formed with low resistance as a desired goal (column 1, lines 38-57). Yoshida et al. (USPN 6,580,143 B2, hereinafter referred to as the "Yoshida" reference) discloses that gold, silver, and titanium have a low resistance (column 4, lines 11-16). In view of Liauh and Yoshida, it would therefore be obvious to

gold, silver, and titanium as contacts in order to gain the benefit of a low resistance contact.

31. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chau (USPN 6,518,155 B1) in view of Russell et al. (USPN 5,648,175).

32. In reference to claim 14, Chau does not explicitly disclose the use of a low dielectric constant interlayer dielectric. However the use of such a material is well known in the art. Russell (USPN 5,648,175) discloses that BPSG (borophosphosilicate glass) is desirable for use as an interlayer dielectric since it has the benefits of a low dielectric constant, low stress, and good adhesion properties (column 1, lines 27-30). Russell discloses that these qualities are desirable in the art (column 1, lines 41-44). In view of Russell, it would therefore be obvious to use a low dielectric constant interlayer dielectric in the device of Chau in order to attain these benefits.

33. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chau (USPN 6,518,155 B1) in view of Sekiguchi (USPN 6,333,255 B1).

34. In reference to claim 14, Chau does not explicitly disclose the use of a low dielectric constant interlayer dielectric. However the use of such a material is well known in the art. Sekiguchi (USPN 6,333,255 B1) discloses that low dielectric constant materials, such as HSQ and Teflon-AF, are desirable for use as an interlayer dielectric since it has the benefits of a low dielectric constant which leads to the possibility of a smaller device (column 1, lines 35-46). The attainment of a smaller semiconductor device is a known goal in the art (column 1, lines 10-15). In view of Sekiguchi, it would

therefore be obvious to use a low dielectric constant interlayer dielectric in the device of Chau in order to attain these benefits.

35. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chau (USPN 6,518,155 B1) in view of Liauh (USPN 5,027,185) and further in view of Wald et al. (USPN 5,932,491).

36. In reference to claim 15, figures 3-5 of Chau each illustrate an integrated circuit which uses a contact for the source/drain junctions (7). Chau does not disclose the exact material which is used for the contact. However Liauh (USPN 5,027,185) discloses that in the semiconductor art, contacts are formed with low resistance as a desired goal (column 1, lines 38-57). Wald et al. (USPN 5,932,491, hereinafter referred to as the "Wald" reference) discloses the use of titanium, tungsten, and alloys thereof in a contact since they have a low resistance (column 5, lines 45-48). In view of Liauh and Wald, it would therefore be obvious to use titanium, tungsten, and its alloys as contacts in order to gain the benefit of a low resistance contact.

37. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chau (USPN 6,518,155 B1) in view of Liauh (USPN 5,027,185) and further in view of Yoshida et al. (USPN 6,580,143 B2).

38. In reference to claim 15, figures 3-5 of Chau each illustrate an integrated circuit which uses a contact for the source/drain junctions (7). Chau does not disclose the exact material which is used for the contact. However Liauh (USPN 5,027,185) discloses that in the semiconductor art, contacts are formed with low resistance as a desired goal (column 1, lines 38-57). Yoshida et al. (USPN 6,580,143 B2, hereinafter

referred to as the "Yoshida" reference) discloses that gold, silver, and titanium have a low resistance (column 4, lines 11-16). In view of Liauh and Yoshida, it would therefore be obvious to gold, silver, and titanium as contacts in order to gain the benefit of a low resistance contact.

Double Patenting

39. Applicant is advised that should claim 1 be found allowable, claim 6 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

40. Applicant is advised that should claim 3 be found allowable, claim 8 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

41. Applicant is advised that should claim 4 be found allowable, claim 9 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing

one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

42. Applicant is advised that should claim 5 be found allowable, claim 10 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Allowable Subject Matter

43. Claims 16 and 18-24 are allowed.

44. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests a field effect transistor having a silicided gate, as well as silicided source and drain regions, with multi-layer spacers which have an outer edge which is aligned with the sidewall of a trench.

Conclusion

45. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

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